PATENT ABSTRACTS OF JAPAN

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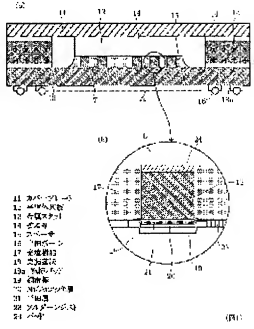
(54) SEMICONDUCTOR ELEMENT, MANUFACTURING METHOD THEREFOR AND SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent the malfunction of a semiconductor integrated circuit due to a soft error even when a metallic bump is formed right below the active layer of a semiconductor element.
SOLUTION: A pad 24 connected to an internal circuit is formed on the active element surface of a semiconductor substrate 12 and a metal stud 13 composed of Cu, Sn-Cu alloy or Sn-Ag alloy is formed on the pad 24 with the film thickness of 20 μm or more. The metal stud 13 is electrically connected through a solder layer 21 to an Ni/Au plating layer 20 on the surface of a copper electrode 21 formed at a recessed part on a mounted substrate 18. Then, filling resin 17 is filled between the semiconductor substrate 12 and the mounted substrate 18, and a part other than the copper electrode 21 is covered with solder resist 23. Thus, since the metal stud 13 is formed of a material not containing lead and the height is turned to be 20 μm or more, the generation of the soft error is suppressed.



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